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10/053,910	01/24/2002	Tomoyuki Furuhata	15.58/6459	3803

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/053,910	Applicant(s) FURUHATA, TOMOYUKI
	Examiner Tu-Tu Ho	Art Unit 2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☒ Claim(s) *17 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The title of the invention is not descriptive (there are more than 270 **thousands** patented inventions having "semiconductor device" in the title). A new title is required that is clearly indicative of the invention to which the claims are directed. The examiner suggests that the title be changed to "Semiconductor Device Having Contact Pads and Method of Manufacturing The Same ".

Drawings

3. The drawings are objected to under 37 CFR 1.81 and 37 CFR 1.83(b) because they are incomplete.

Claims 23 and 21 and dependent claim 22 draw to a semiconductor device and method of manufacturing thereof comprising a reflection prevention film, which is not shown in the figures, on the upper level wiring.

The claimed feature requires an illustration by a drawing to facilitate understanding.

A proposed drawing correction or corrected drawings are required in reply to the Office action.

Claim Objections

4. Correct the typographical errors in claims 17 and 20 that the examiner has enclosed in brackets ([]) in the rejection section below.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

6. Claims 5-7, 12-16, and 23 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites: "a second wiring layer that provides a pad section formed above the first wiring layer through a *second interlayer insulation layer*", claim 6 recites: "the upper surface of the first interlayer insulation layer further comprises a second region where the pad opening section is formed vertically thereabove, and at least part of the second interlayer insulation layer is formed on the second region", and claim 13 recites: "first wiring layer is only formed on the first region and the *second interlayer insulating layer is formed over the entire second region*". It is clear from the figures that the second interlayer insulating layer is not formed on the second region. As best as can be understood, device claims 5-7, 12-16, and 23 are basically the same as method claims 17-22 and will be treated as such.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
>
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

8. Claims 1-5, 7-11, and 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Freeman, Jr. et al. U.S. Patent 5,149,674.

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Freeman discloses in the single figure and respective portions of the specification a semiconductor device and method of manufacturing thereof as claimed.

Referring to claims 1 and 8, Freeman discloses a semiconductor device (and an inherent method of manufacturing thereof) comprising:

a protective insulation layer 28;

a pad opening section (defined by the opening of layer 28) provided in the protective insulation layer;

a wiring layer 27 which the pad opening section reaches; and

a wiring layer 13/18 provided at a level lower than the wiring layer which the pad opening section reaches, wherein the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

Regarding claims 2 and 9, Freeman further discloses that wiring layer 27 which the pad opening section reaches is composed of one layer.

Regarding claims 3 and 10, Freeman further discloses that wiring layer 27/23 which the pad opening section reaches is composed of two layers.

Referring to claims 4 and 11, it is evident from the figure that wiring layer 27 which the pad opening section reaches has a thickness that is greater than that of the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches.

With respect to claim 5, Freeman discloses a semiconductor device comprising:

a first wiring layer 13/18/23 formed above a semiconductor layer through a first interlayer insulation layer 14;

a second wiring layer 27 that provides a pad section formed above the first wiring layer through a second interlayer insulation layer 24;

a protective insulation layer 28 formed above the second wiring layer and the second interlayer insulation layer; and

a pad opening section provided in the protective insulation layer, wherein an upper surface of the first interlayer insulation layer includes a first region where the protective

insulation layer is formed vertically thereabove, and the first wiring layer is formed on the first region.

Referring to claim 7, Freeman further discloses that first wiring layer 13/18/23 includes a plurality of wiring layers in the same layer, and the plurality of wiring layers are formed on the first region.

Referring to claim 15, Freeman further discloses that a third wiring layer 18 positioned between the first wiring layer 13 and the second wiring layer 23; and

a third interlayer insulation layer positioned between the first interlayer insulation layer and the second interlayer insulation layer.

With respect to claim 16, Freeman further discloses that third wiring layer 18 is connected to the first wiring layer 13 through a plurality of first plugs 17 and the third wiring layer is connected to the second wiring layer through a plurality of second plugs 22, and the first plugs and the second plugs are positioned to be offset from each other in a vertical direction (as is evident from the figure).

9. Claims 1-2, 4-6, 8-9, 11-14, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujiki et al. U.S. Patent 5,736,791.

Fujiki discloses in Figures 1-19, specifically Figures 4-6, and respective portions of the specification a semiconductor device and method of manufacturing thereof as claimed.

Referring to claims 1 and 8, Fujiki discloses a semiconductor device (and an inherent method of manufacturing thereof) comprising:

(referring now to Figures 4-6 for an illustration) a protective insulation layer 7;

a pad opening section (defined by the opening of layer 7) provided in the protective insulation layer;

a wiring layer 6 which the pad opening section reaches; and

a wiring layer 3 provided at a level lower than the wiring layer which the pad opening section reaches, wherein the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

Regarding claims 2 and 9, Freeman further discloses that wiring layer 6 which the pad opening section reaches is composed of one layer.

Referring to claims 4 and 11, it is evident from the figure that wiring layer 6 which the pad opening section reaches has a thickness that is greater than that of the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches.

Referring to claims 17 and 5-6, 13, Fujiki discloses a method for manufacturing a semiconductor device, comprising:

forming a lower/first level wiring layer 3;

forming a[n] lower/first level interlayer dielectric layer 4 on and adjacent to the lower/first level wiring layer;

forming an upper/second level wiring layer 6 above the lower/first level interlayer dielectric layer, wherein the lower/first level wiring layer is electrically connected to the upper/second level wiring layer;

forming a protective/second interlayer insulation layer 7 on the upper level wiring layer;

removing a first portion of the protective/second interlayer insulation layer over the upper/second level wiring layer and over the lower/first level interlayer dielectric layer to form a pad opening section of the upper/second level wiring layer, wherein a second portion of the protective insulation layer located vertically above the lower level wiring layer remains after removing the first portion of the protective layer; and

wherein no portion of the lower/first level wiring layer is disposed vertically below the pad opening section .

Referring to claim 14, a portion of the second interlayer/protective insulating layer 7 is formed over the first region.

Regarding claim 12, first wiring layer 3 is only formed on the first region.

10. Claims 1-2, 8-9, 5, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Anand U.S. Patent 6,362,528.

Similarly as detailed above, Anand disclose in Figures 1-45, specifically figure 45, and respective portions of the specification a semiconductor device and method of manufacturing thereof as claimed.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 23, 21, and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Freeman, Jr. et al. or over Fujiki.

Referring to claims 23, 21, and 22, Freeman discloses a semiconductor device and method of manufacturing thereof as claimed and as described above, but fails to discloses a reflection prevention film. However, the addition of another element in Applicant's claimed invention of claims 5 and 17 cannot make the device patentable unless it then performs new or surprising function. No such function has shown for claimed device. See Santa Anita Mfg. Corp. v. Lugash et al., 152 USPQ 44(CA 9 1966). As a general rule, the addition of an element to a patented structure which does not substantially change the function of the patented structure is not patentable. See King-Seeley Thermas Co. v. Refrigerated Dispeners, Inc., 354 F.2d 533,540, 148 USPQ 114, 119-120 (10th Cir. 1965); Hayes Spray Gun Company v. E.C. Brown Company, 291 F.2d 319, 326, 129 USPQ 383, 389 (8th Cir. 1961).

Similarly, referring to claims 23, 21, and 22, Fujiki discloses a semiconductor device and method of manufacturing thereof as claimed and as described above, but fails to discloses a reflection prevention film. However, the addition of another element in Applicant's claimed invention of claims 5 and 17 cannot make the device patentable unless it then performs new or surprising function.

13. Claims 3 and 10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fujiki et al.

Similarly as note above, the limitation "the wiring layer which the pad opening reaches is composed of two layers" of claims 3 and 10 is unpatentable over Fujiki et al. in the guideline that the addition of an element to a patented structure which does not substantially change the function of the patented structure is not patentable. Furthermore, the use of multiple layers for the top most layer which the pad opening reaches is well known in the art, as shown in Figure 11.

14. Claims 18-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fujiki et al. as applied above, in view of Domae et al. U.S. Patent 6,197,685 or in view of Freeman.

Referring to claims 7, 15, 16, 18 and 20, Fujiki discloses a semiconductor device and method of manufacturing thereof as claimed and as described above, but fails to discloses that there exists an intermediate wiring layer and an intermediate interlayer dielectric layer; wherein the intermediate wiring layer is positioned above the lower level wiring layer and below the upper level wiring layer; and the intermediate interlayer dielectric layer is positioned above the lower level interlayer dielectric layer and below the upper level wiring layer. Fujiki also fails to disclose:

the lower level wiring layer to be electrically connected to the intermediate level wiring layer;

forming the intermediate level wiring layer to be electrically connected to the upper level wiring layer;

forming the lower level wiring layer to include [has] a thickness that is less than that of the lower level interlayer dielectric layer;

forming the intermediate level wiring layer to include a thickness that is less than that of the intermediate level interlayer dielectric layer;

forming a plurality of lower level plugs to electrically connect the lower level wiring layer to the intermediate level wiring layer;

forming a plurality of intermediate level plugs to electrically connect the intermediate level wiring layer to the upper level wiring layer; and

wherein the intermediate plugs are formed to be offset from the lower level intermediate plugs in a vertical direction.

Nevertheless, the use of contact pad structure having multiple level wirings wherein conductive plugs at different levels for electrically connecting wirings of different wiring levels are offset in a vertical direction is well known in the art. Domae discloses in the patent entitle Method of producing multilayer wiring device with offset axises of upper and lower plugs that: "A multilayer wiring structure of a semiconductor device having a stacked structure is arranged to restrain reliability degradation due to stress applied to the region of wiring between opposite upper and lower plugs. The rate of overlap of contact surface between upper plug and wiring on contact surface between lower plug and wiring, is small to the extent that no void is generated. The multilayer wiring structure is produced such that no grain boundary is contained in the region of wiring between upper and lower plugs"; and Freeman teaches "in a preferred embodiment, vias 22 are staggered or offset so that vias 22 are not stacked on vias 17. This offsetting of vias 17 and 22 allows for easier processing. However, stacking of vias 17 and 22 can be done" (column 4, lines 40-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a structure and method as claimed in

claims 18 and 20. One would have been motivated to make such a modification in view of the suggestion in Domae and Freeman for the reasons cited.

Regarding claims 7 and 19, the Fujiki's structure and method modified as described above would entail that no portion of the intermediate lower level wiring layer is disposed vertically below the pad opening section.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent 4,984,061 to Matsumoto discloses a semiconductor device in which wiring layer is formed below bonding pad.

b. U.S. Patent 5,700,735 to Shiue et al. discloses a method for forming bond pad structure wherein via plugs for connecting the three metal pads of the bond pad structure are formed in a diamond shape.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (703) 305-0086. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Tu-Tu Ho
September 20, 2002

HOAI HO
PRIMARY EXAMINER